

Fig. 1

Fig. 2

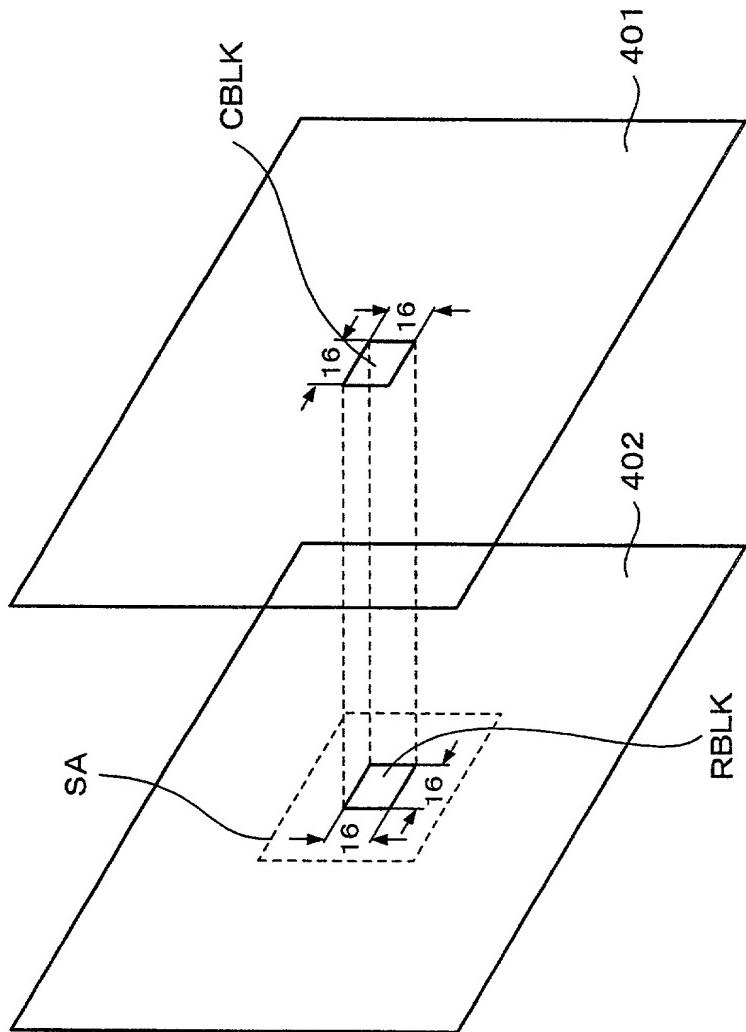


Fig. 3

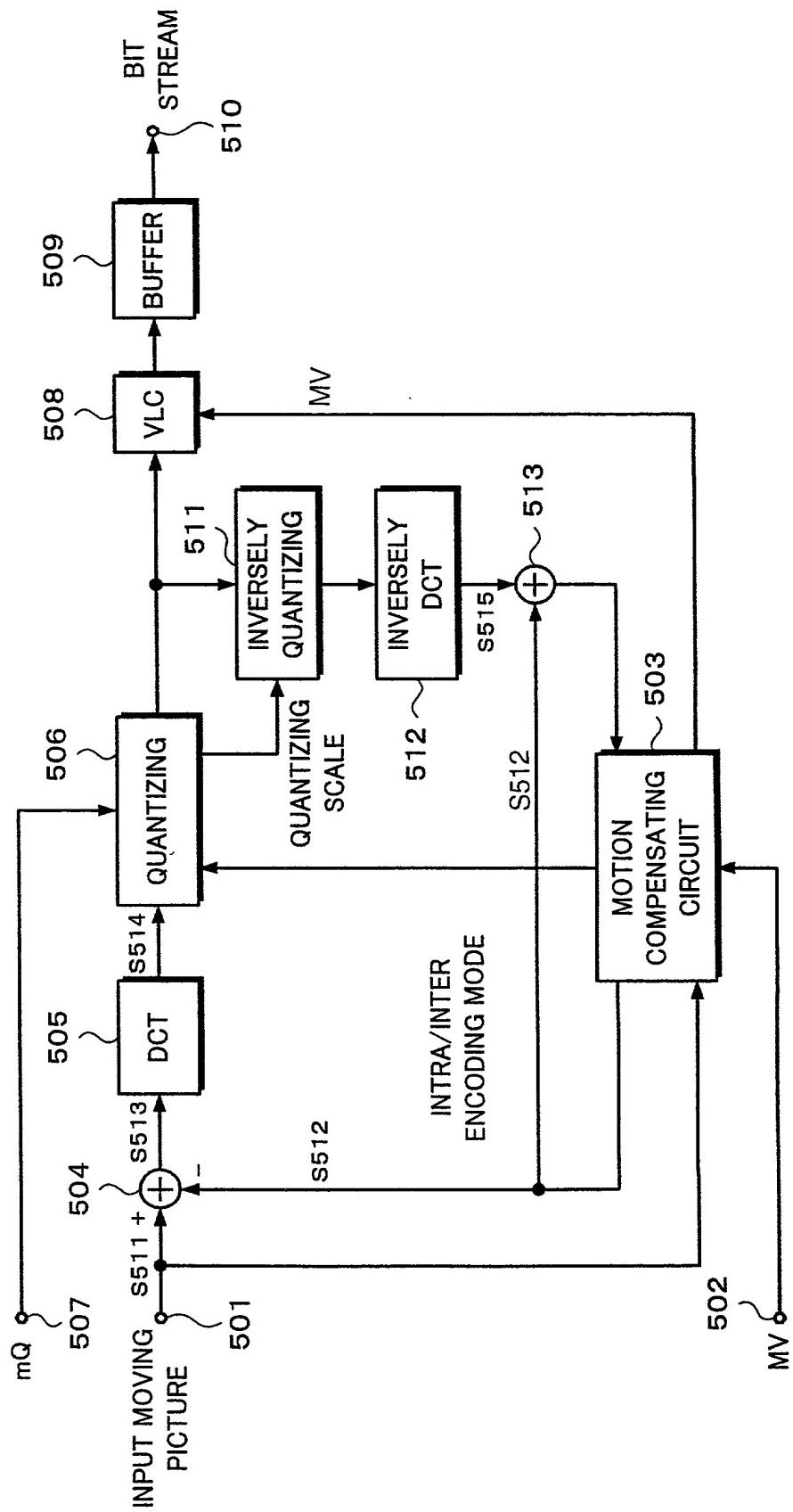


Fig. 4

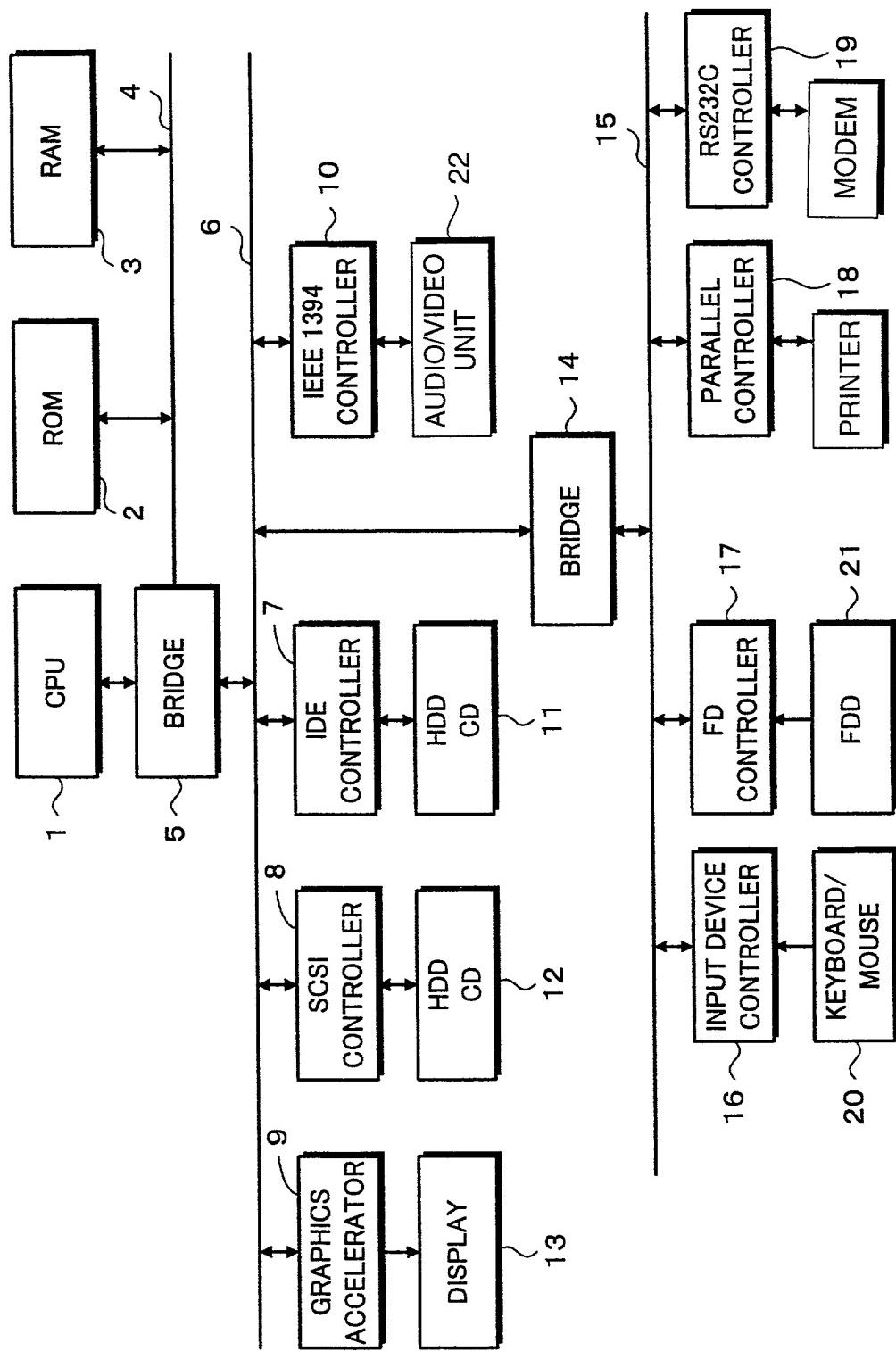


Fig. 5

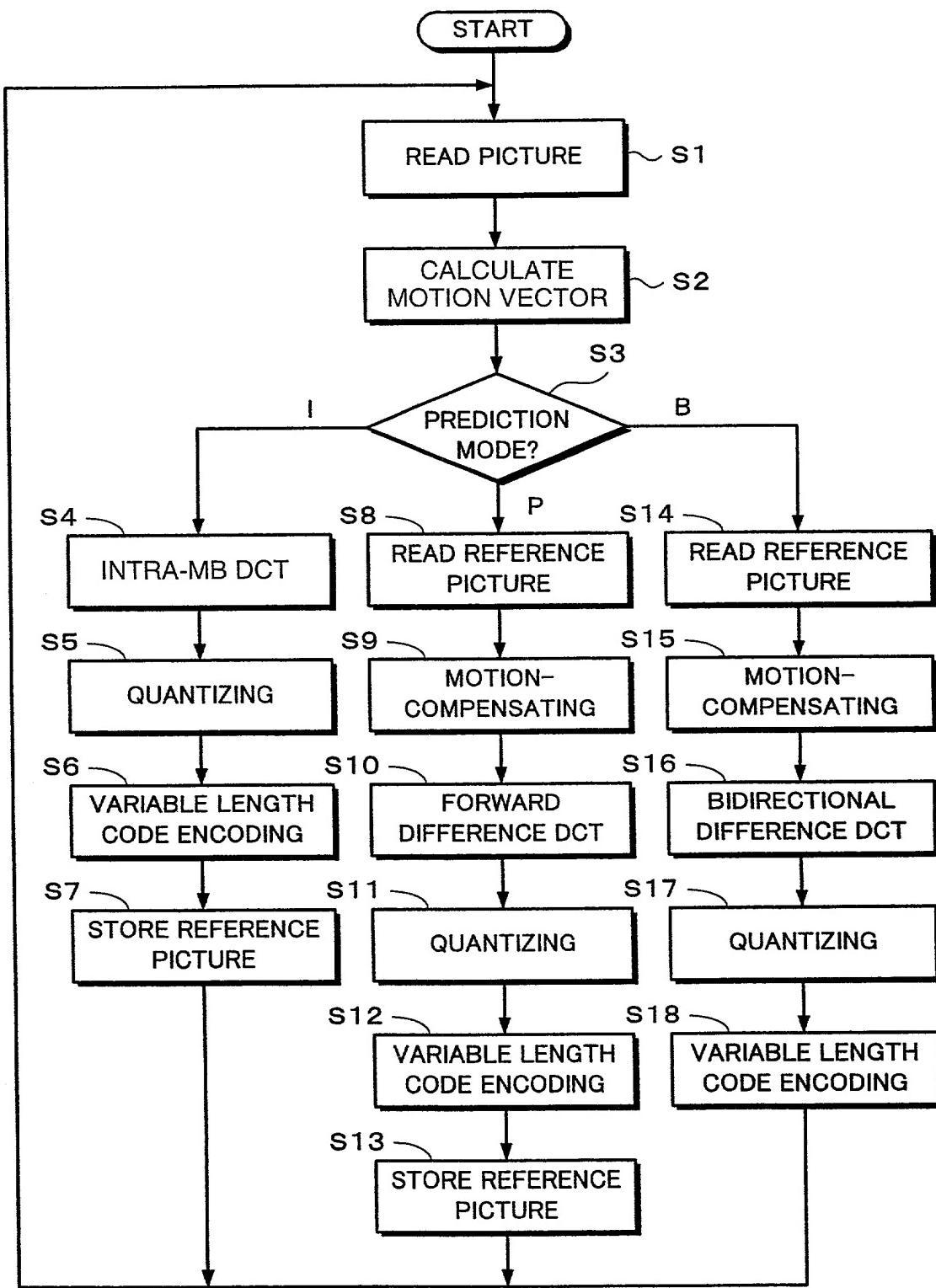


Fig. 6

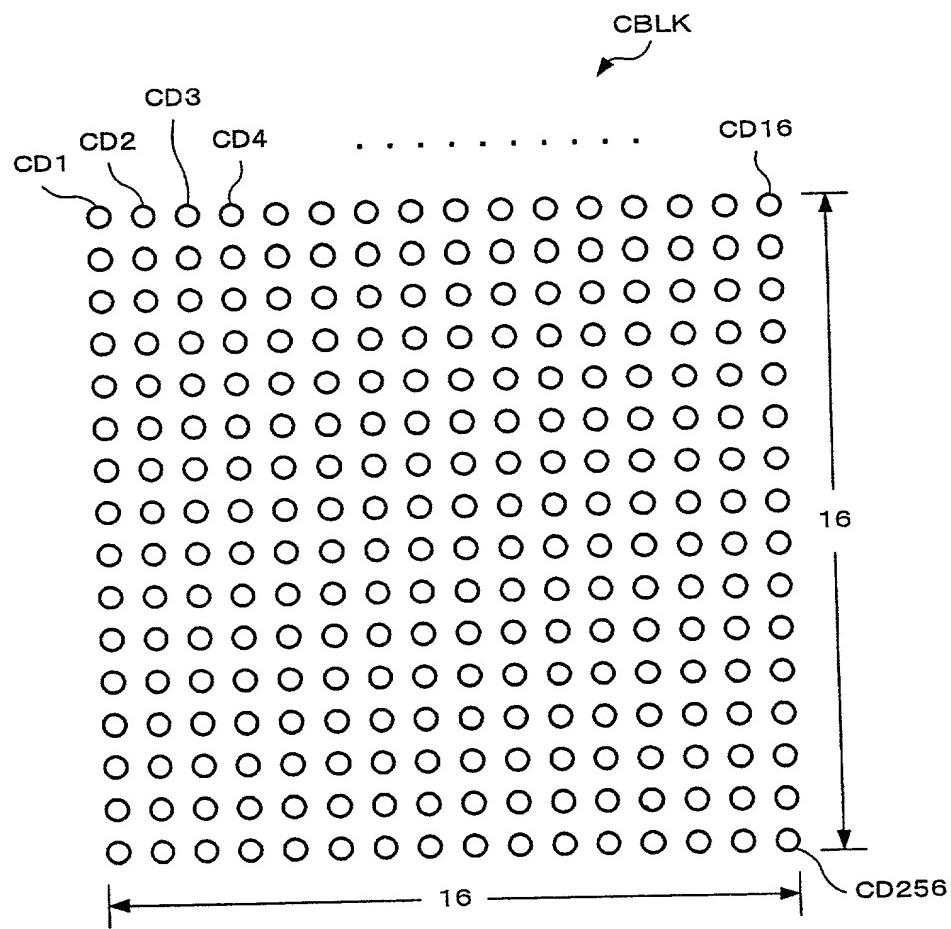


Fig. 7

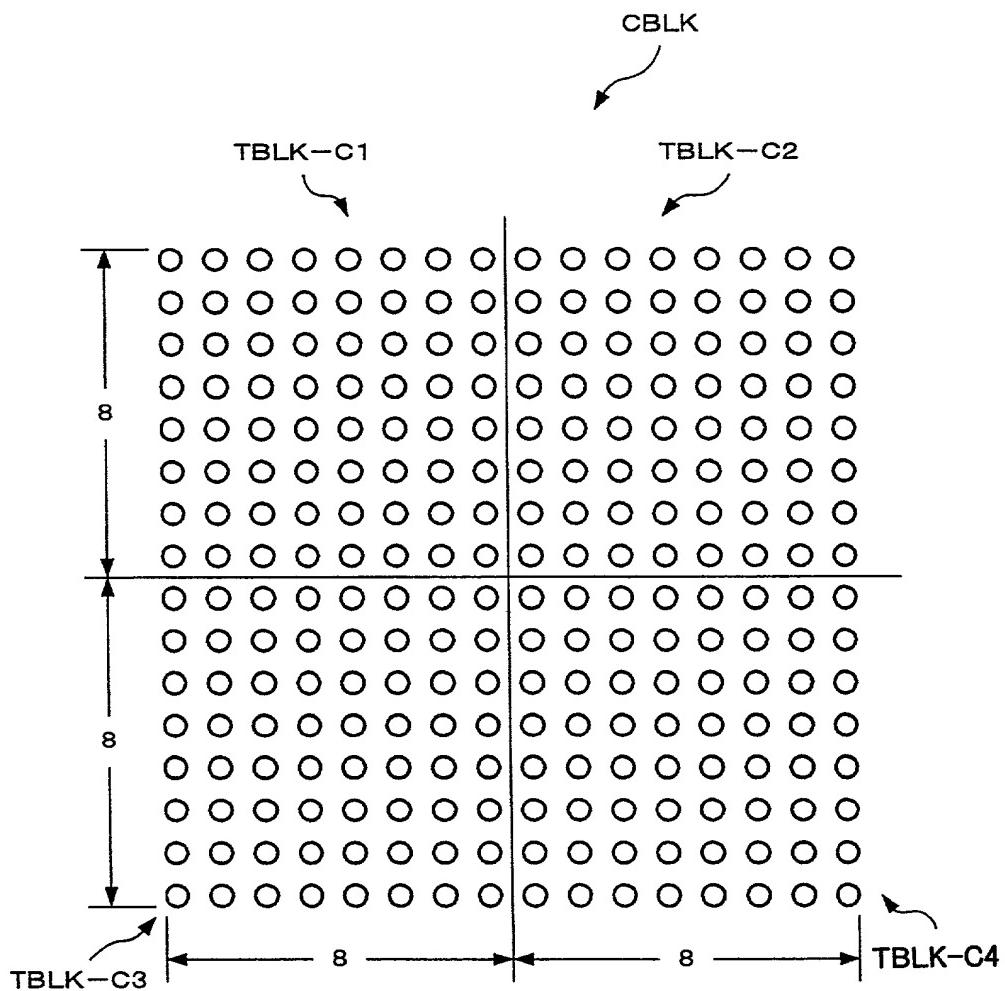


Fig. 8

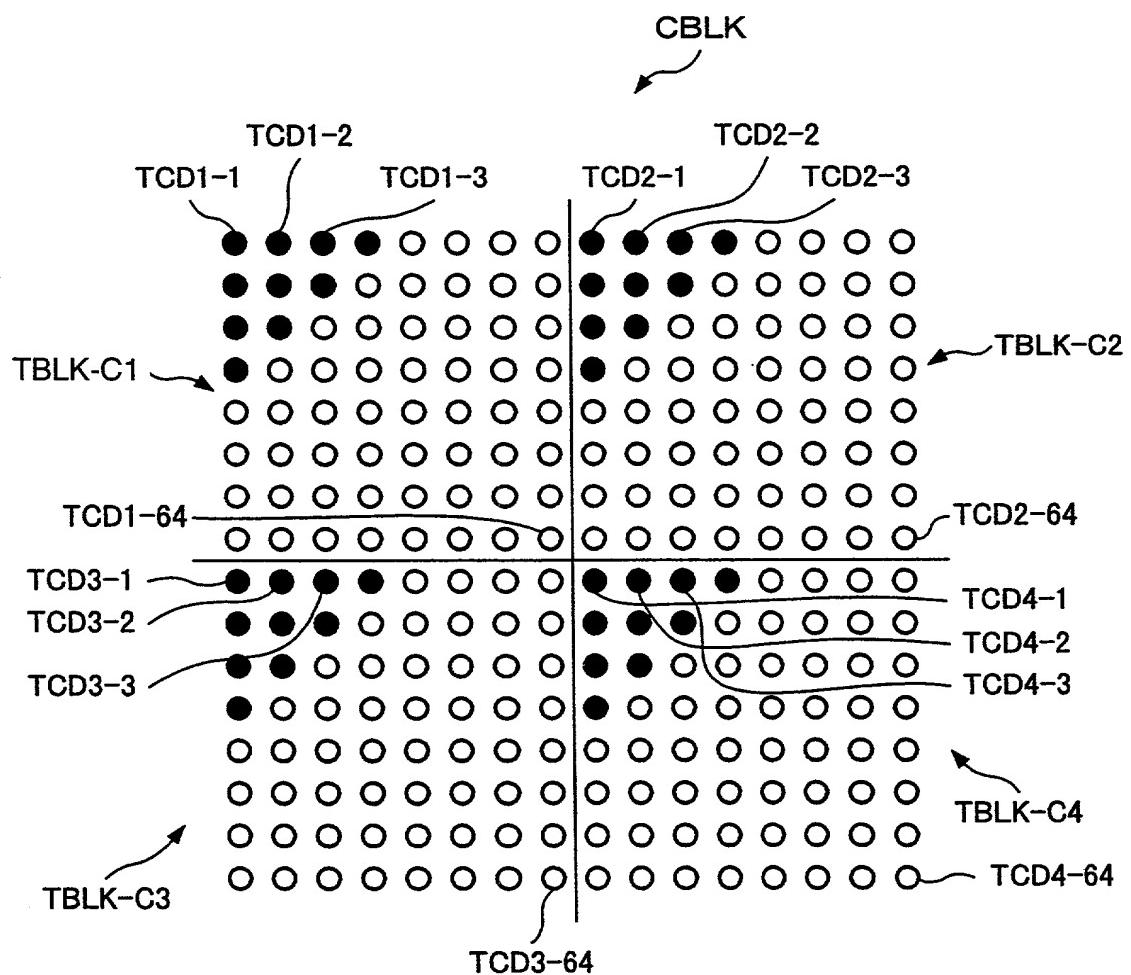


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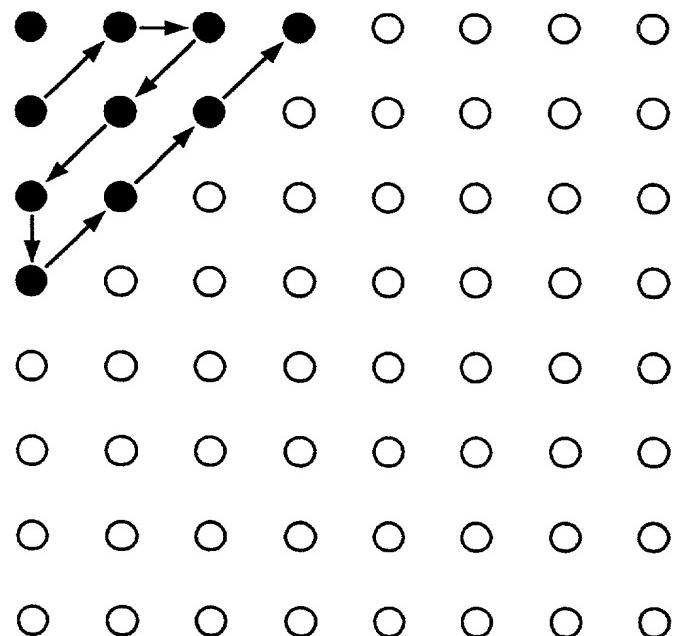


Fig. 10

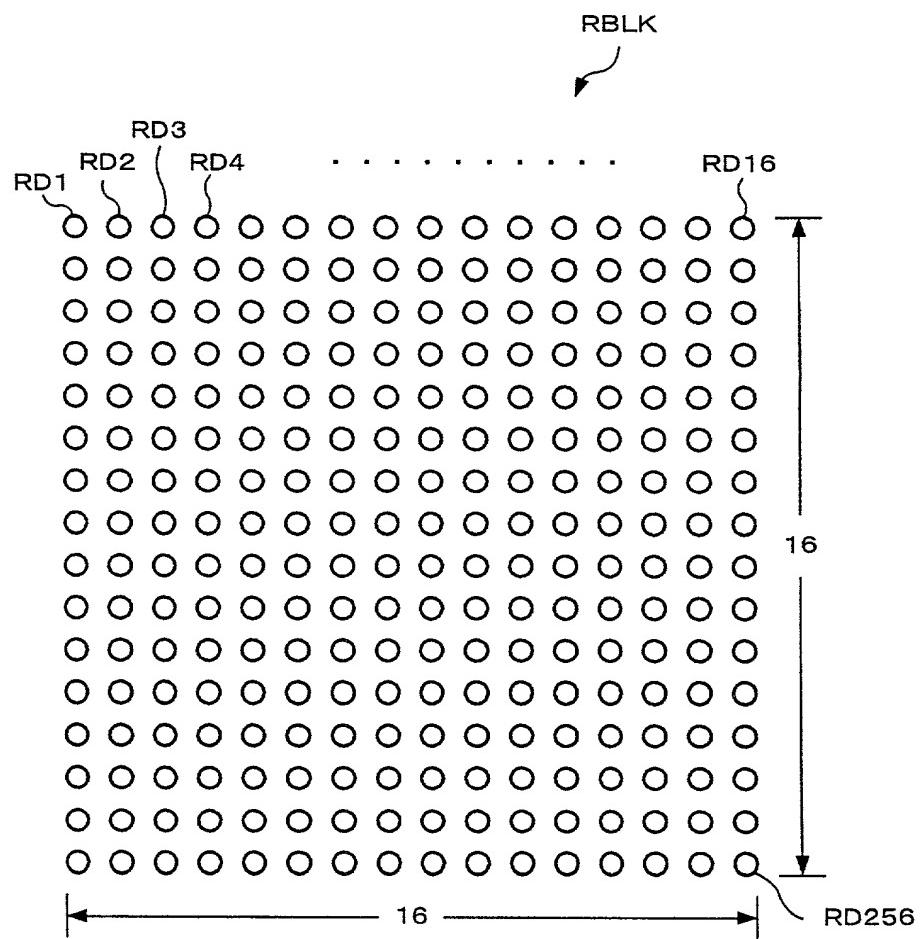


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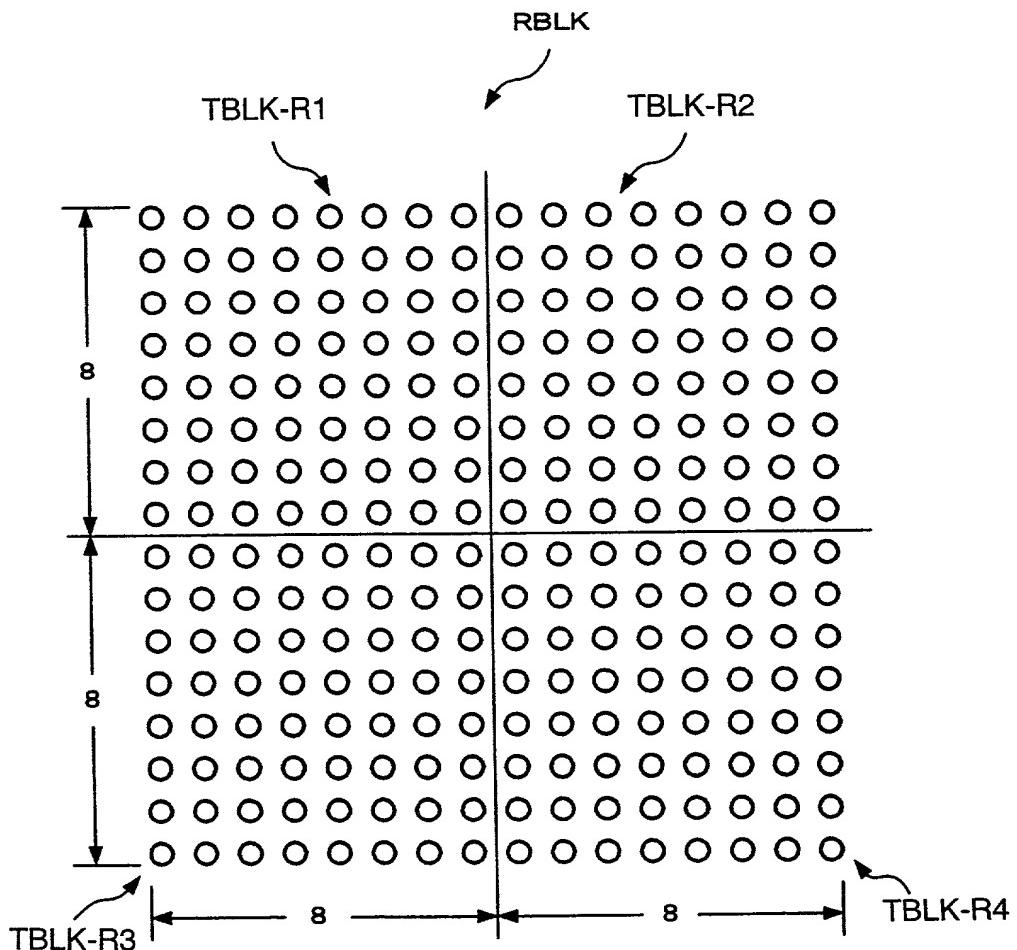


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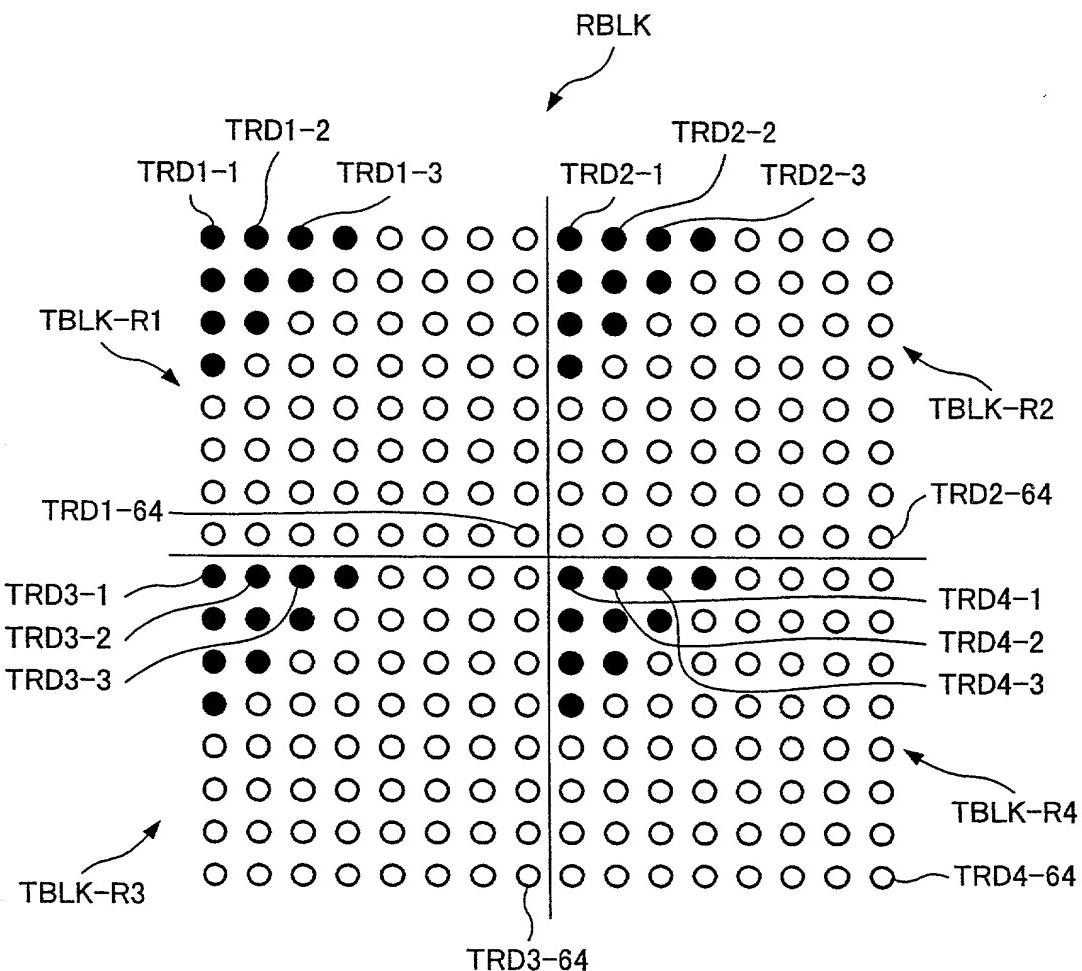


Fig. 13

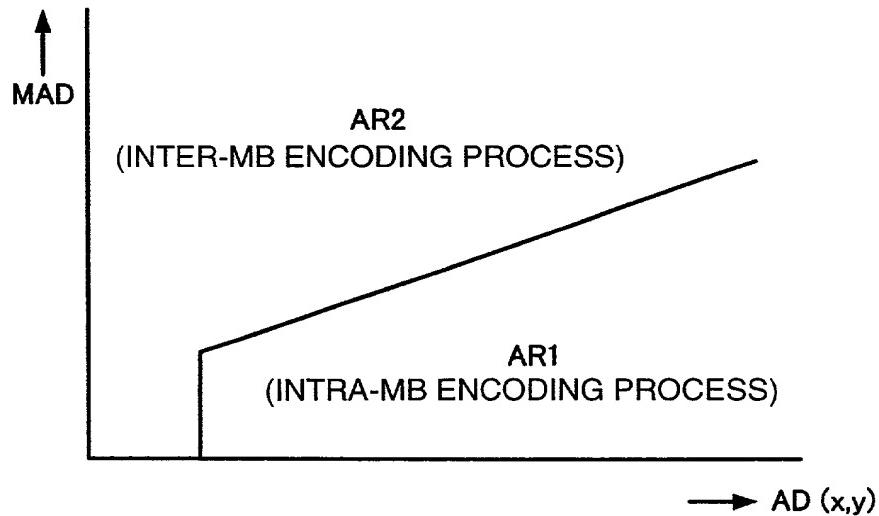


Fig. 14

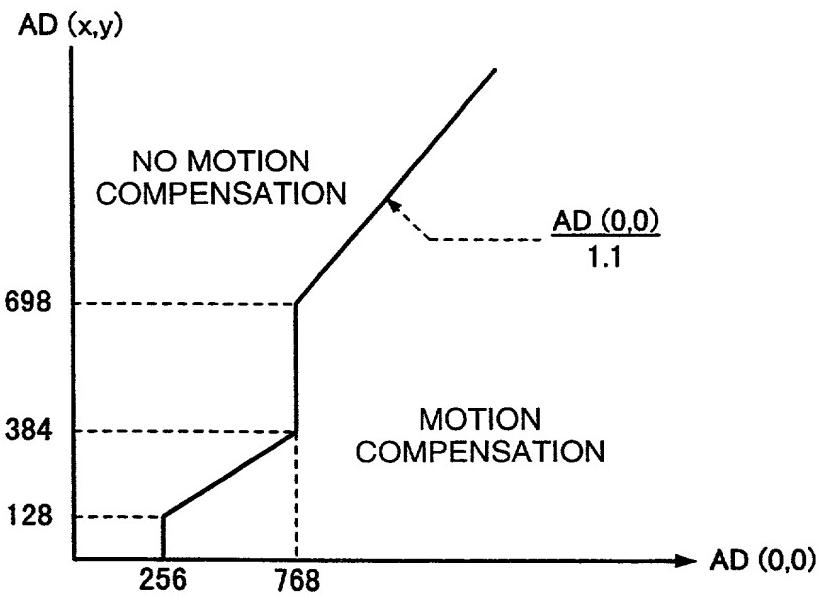


Fig. 15

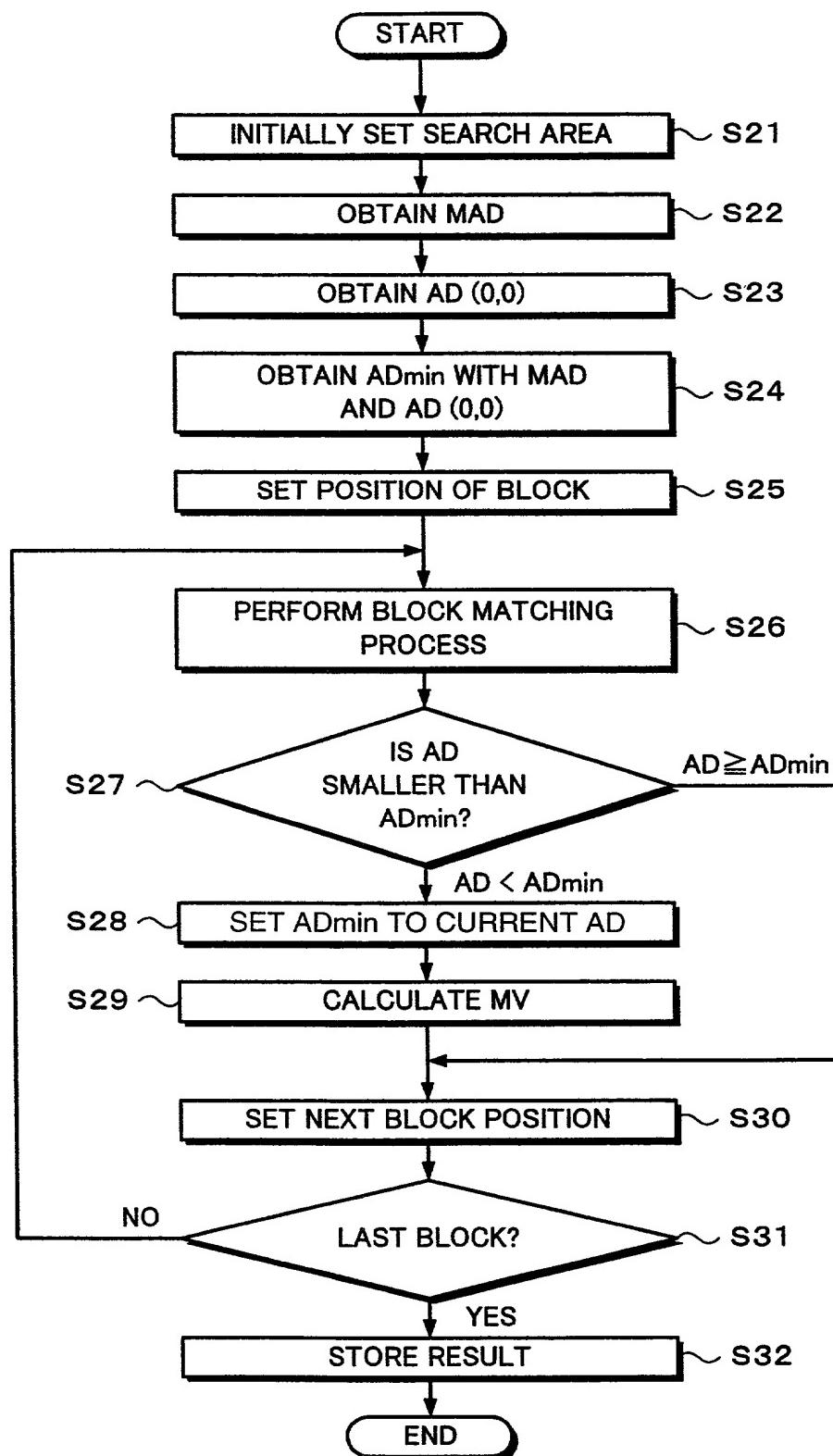


Fig. 16

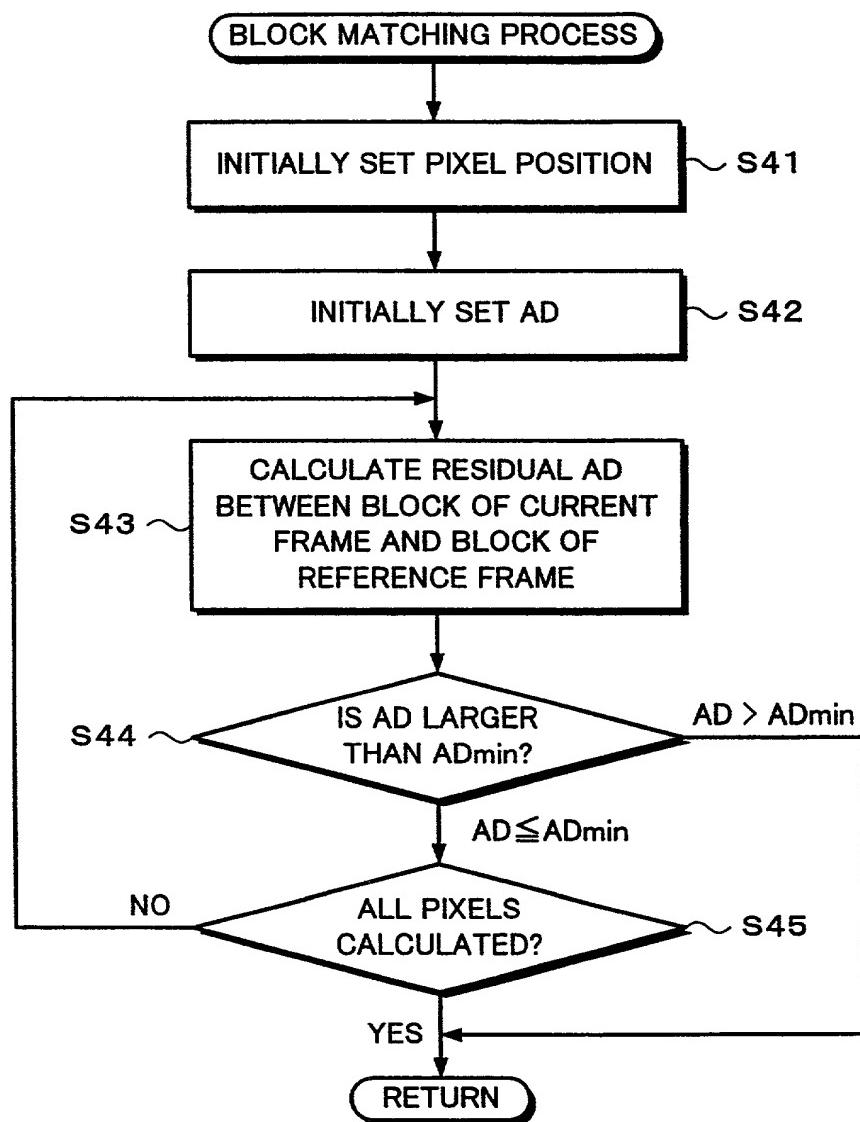


Fig. 17

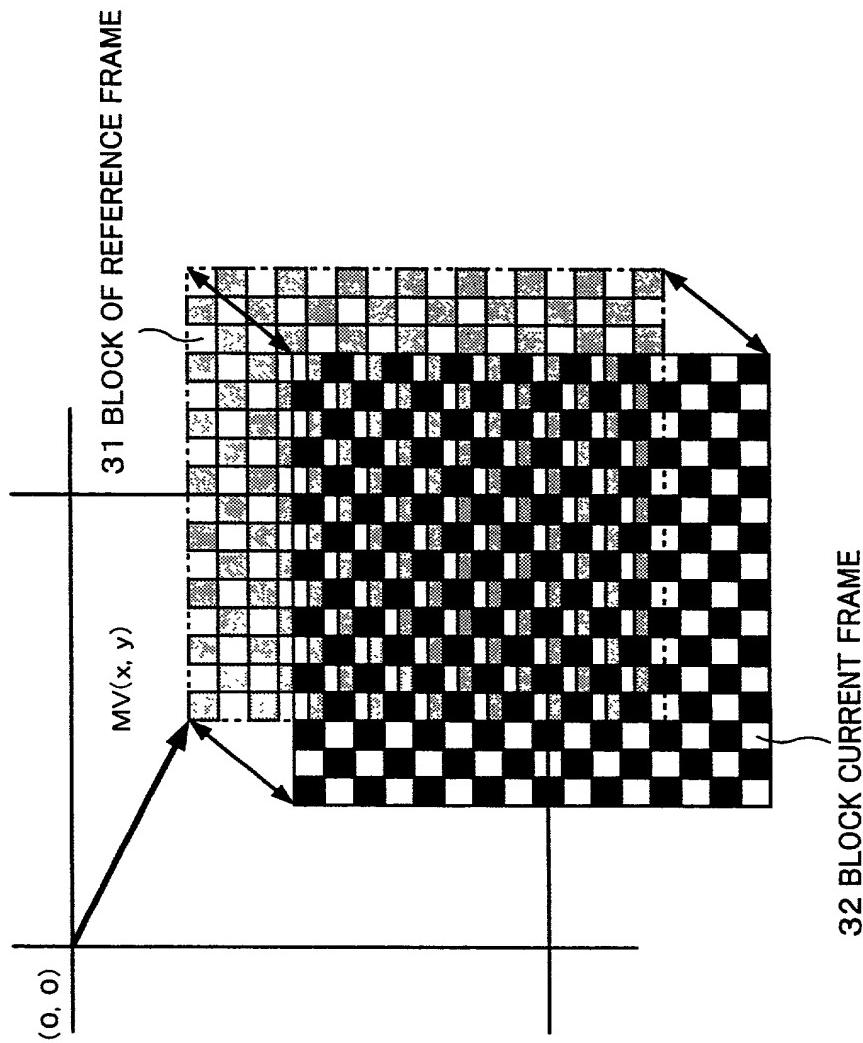


Fig. 18A

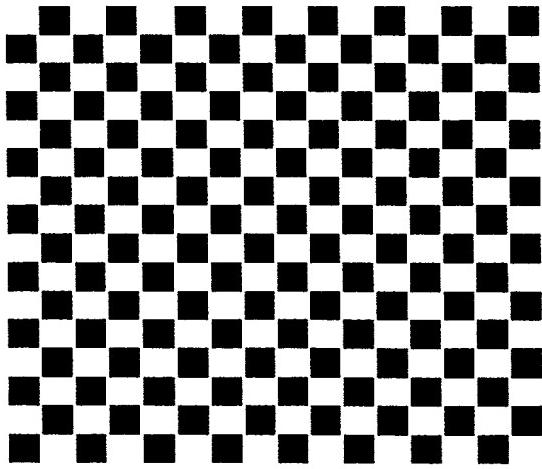


Fig. 18B

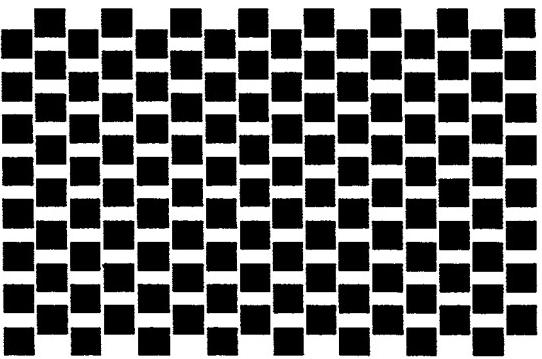


Fig. 18C

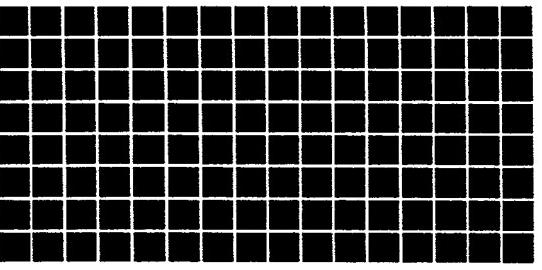


Fig. 19A

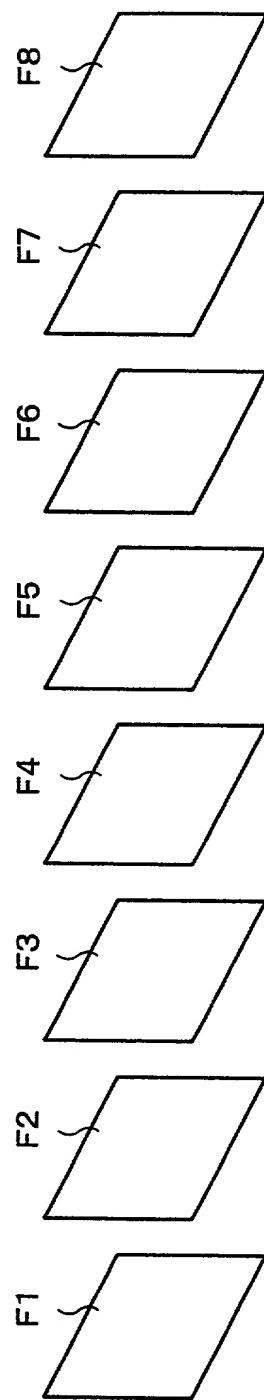


Fig. 19B

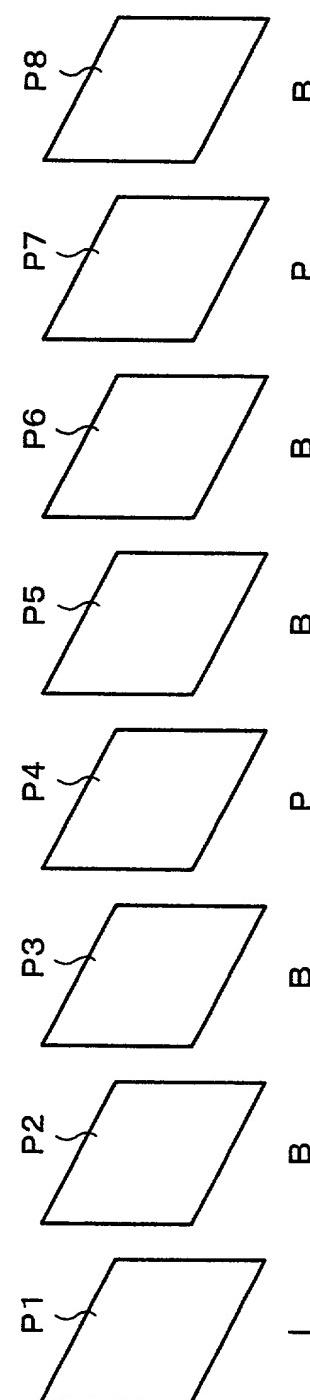


Fig. 20

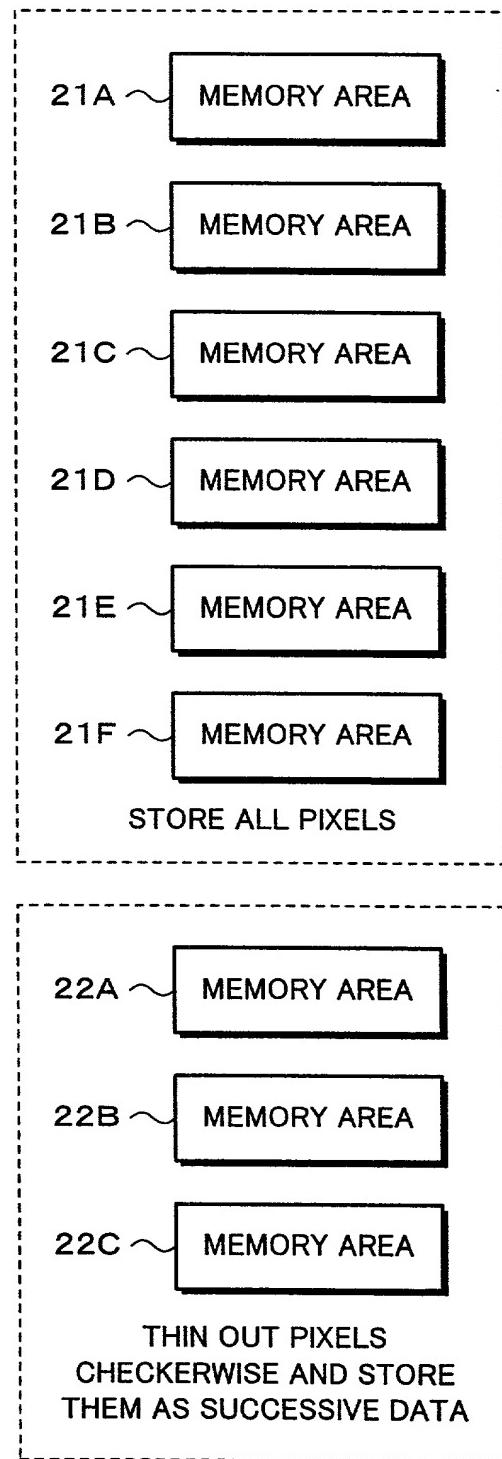


Fig. 21

TIME POINT	T1	T2	T3	T4	T5	T6	T7	T8	T9
MEMORY AREA 21A	F1	F1	F1	F1	F1	F1	F7	F7	F7
MEMORY AREA 21B		F2	F2	F2	F2	F2	F8	F8	
MEMORY AREA 21C			F3	F3	F3	F3	F3	F9	
MEMORY AREA 21D				F4	F4	F4	F4	F4	F4
MEMORY AREA 21E					F5	F5	F5	F5	F5
MEMORY AREA 21F						F6	F6	F6	F6
MEMORY AREA 22A				f1	f1	f1	f7	f7	f7
MEMORY AREA 22B				f4	f4	f4	f4	f4	f4
MEMORY AREA 22C					f2	f3	f3	f5	f6
OPERATION	ENCODE P1			ENCODE P4	ENCODE P2	ENCODE P3	ENCODE P7	ENCODE P5	ENCODE P6

Fig. 22

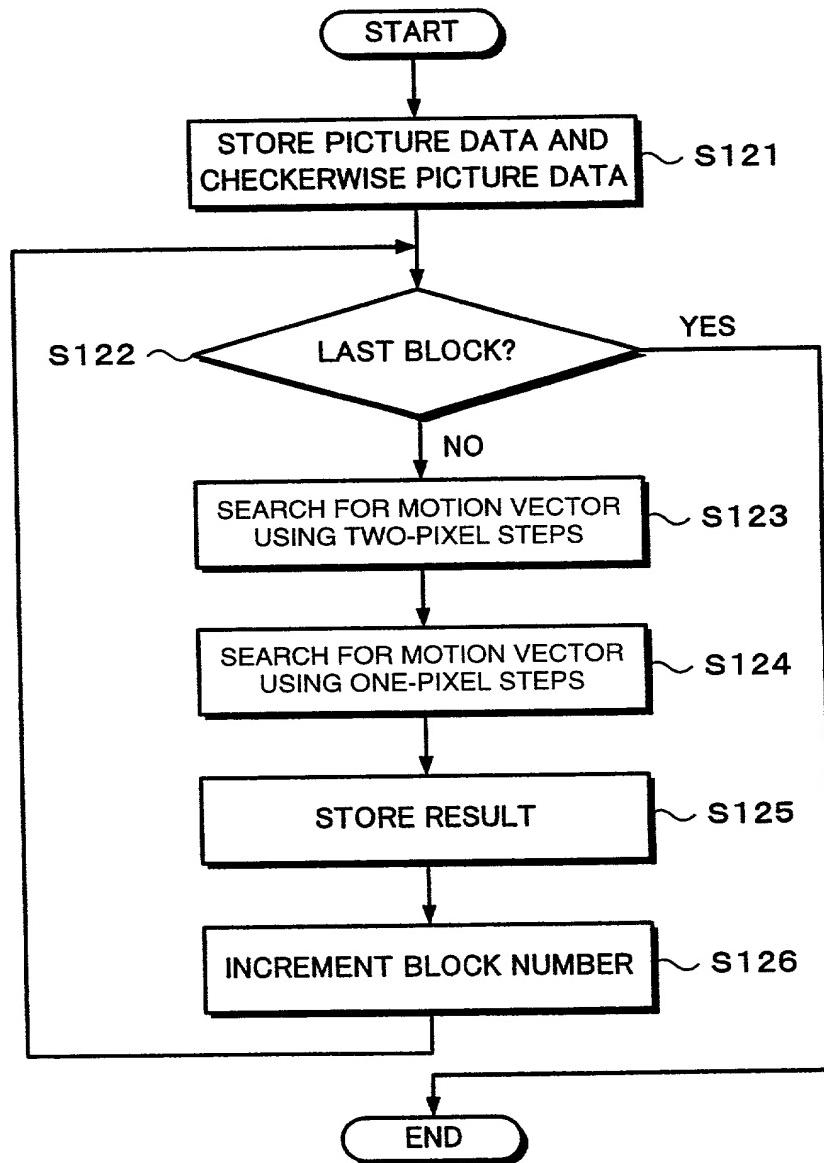


Fig. 23

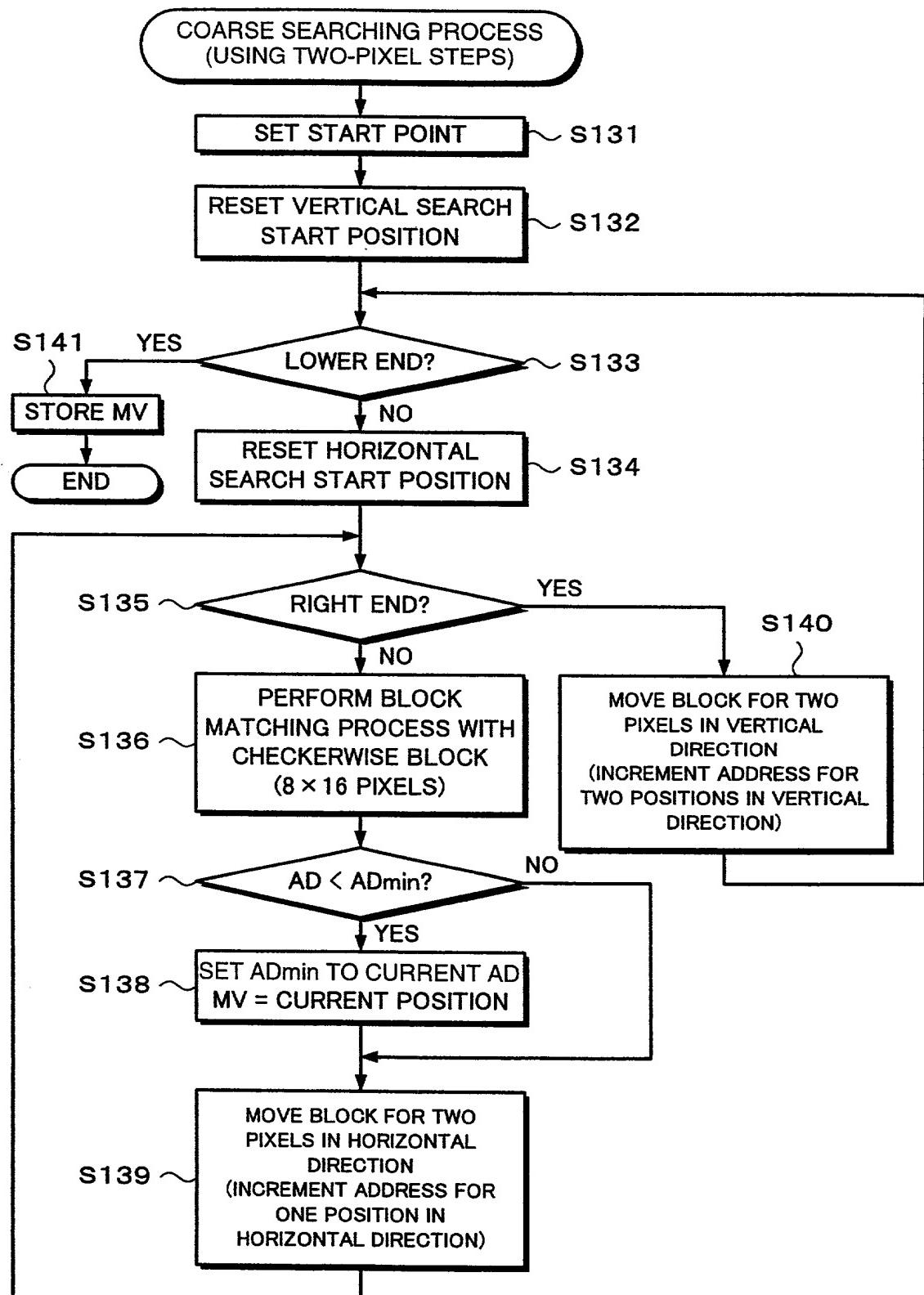


Fig. 24

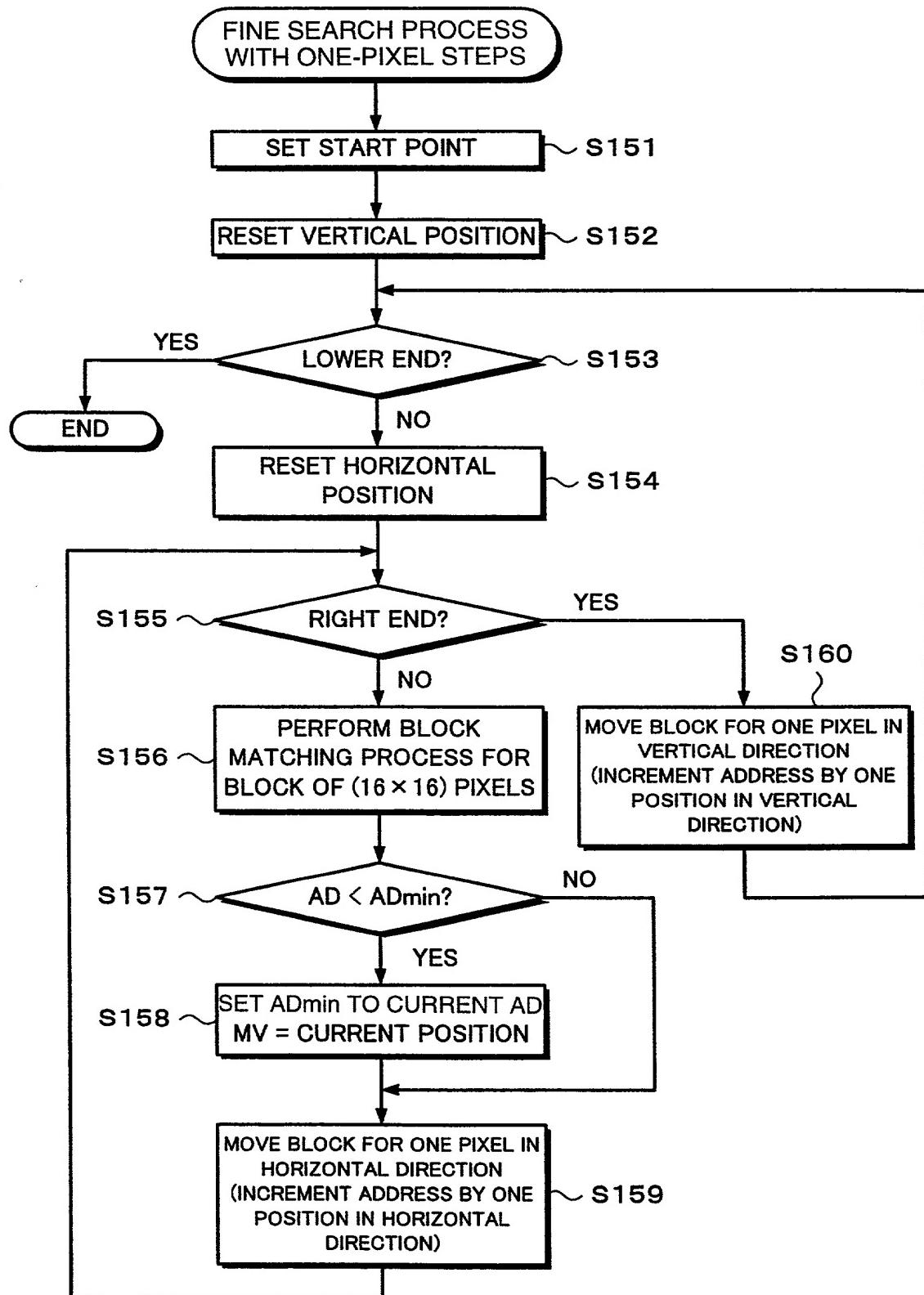


Fig. 25

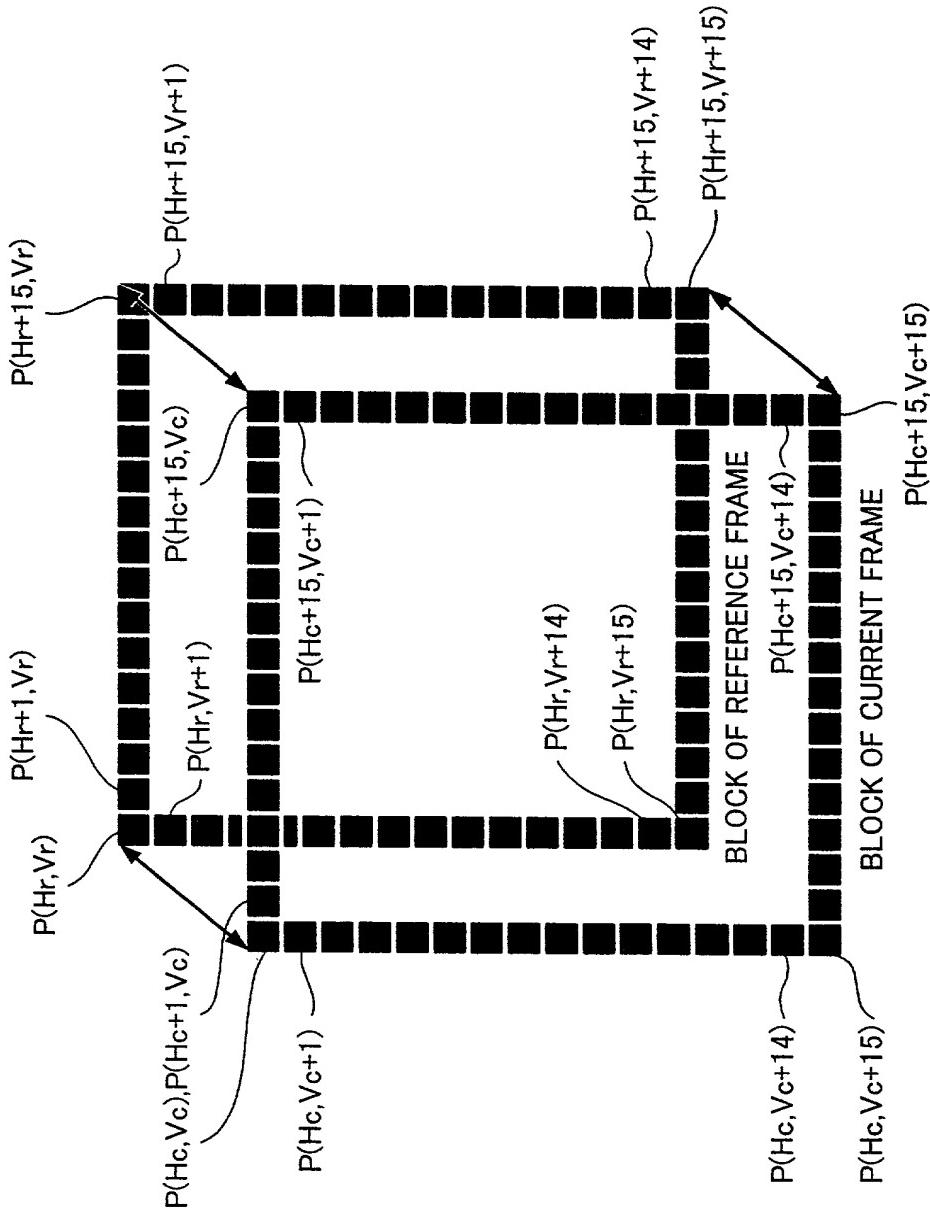


Fig. 26

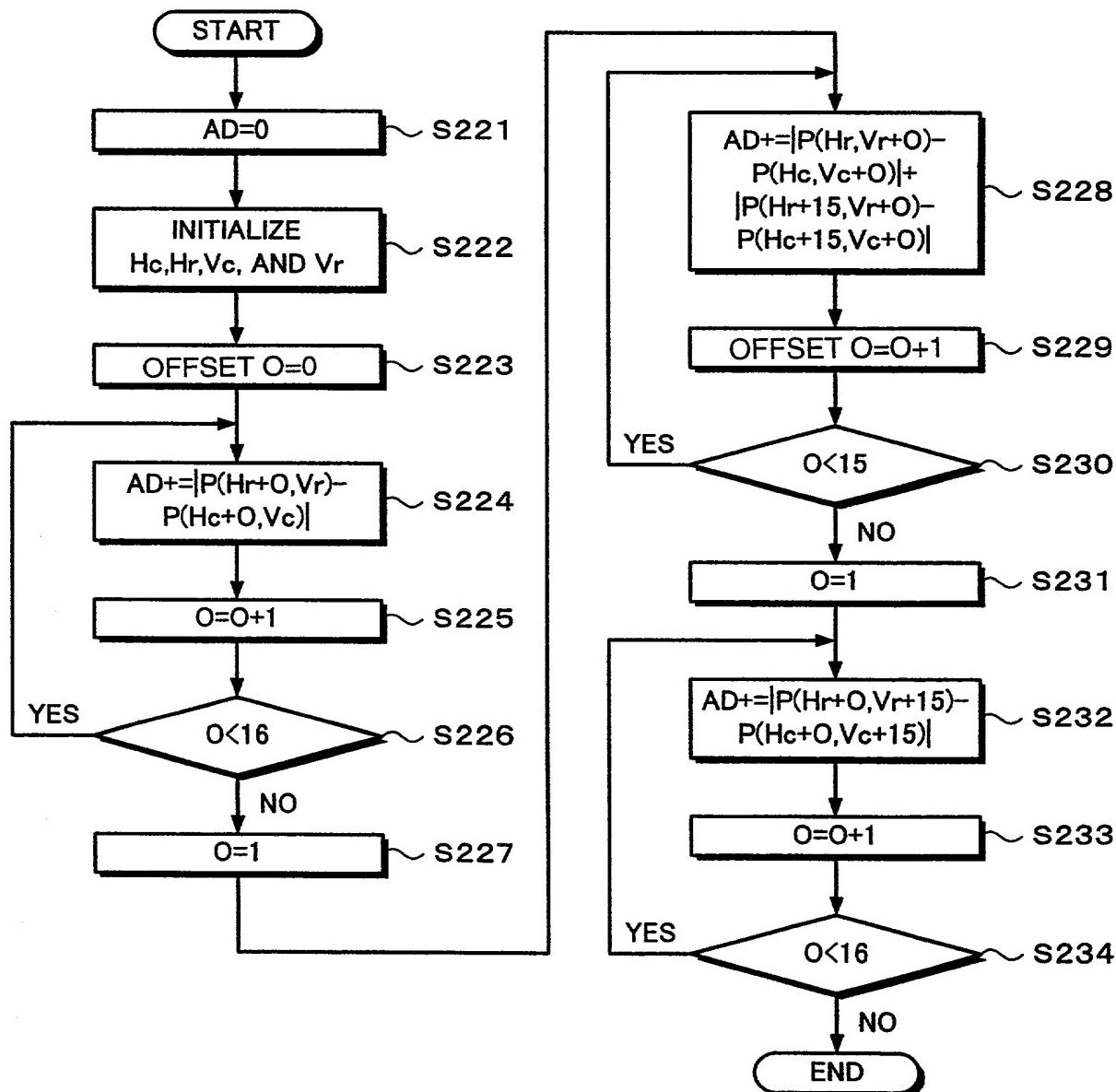


Fig. 27

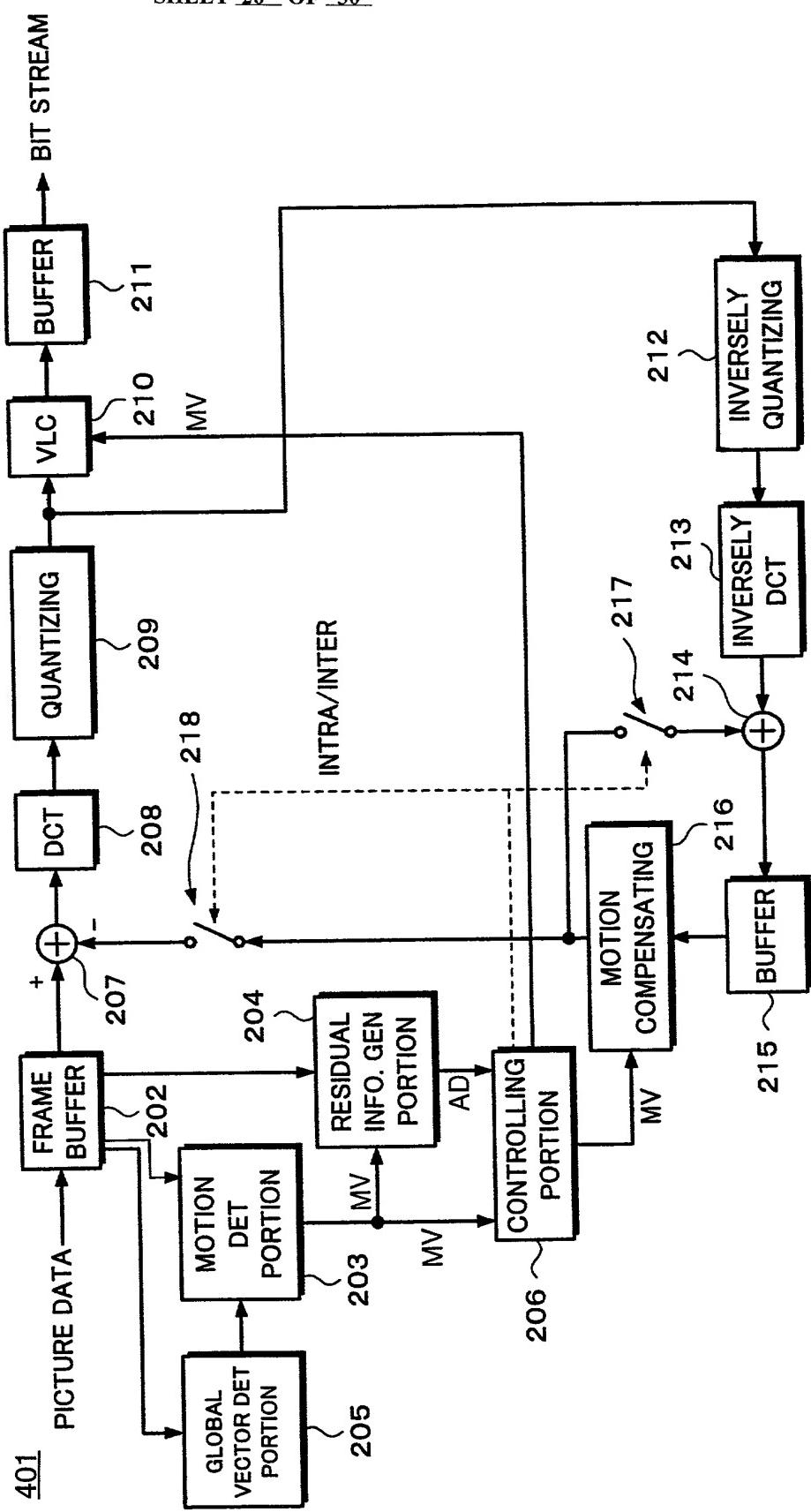


Fig. 28

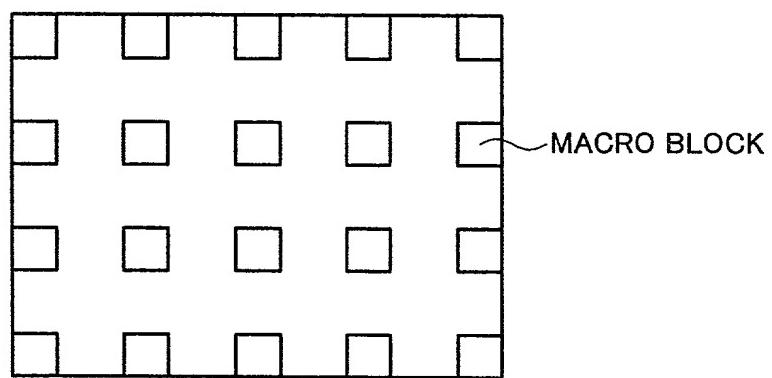


Fig. 29

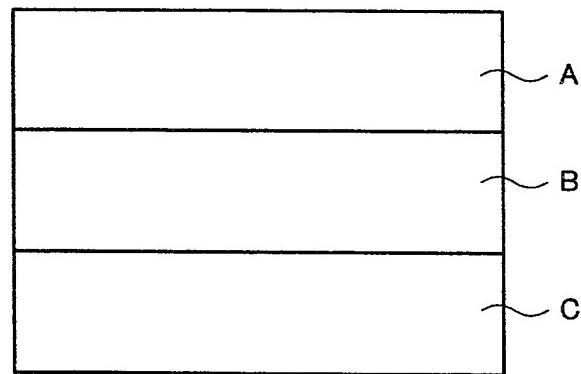


Fig. 30

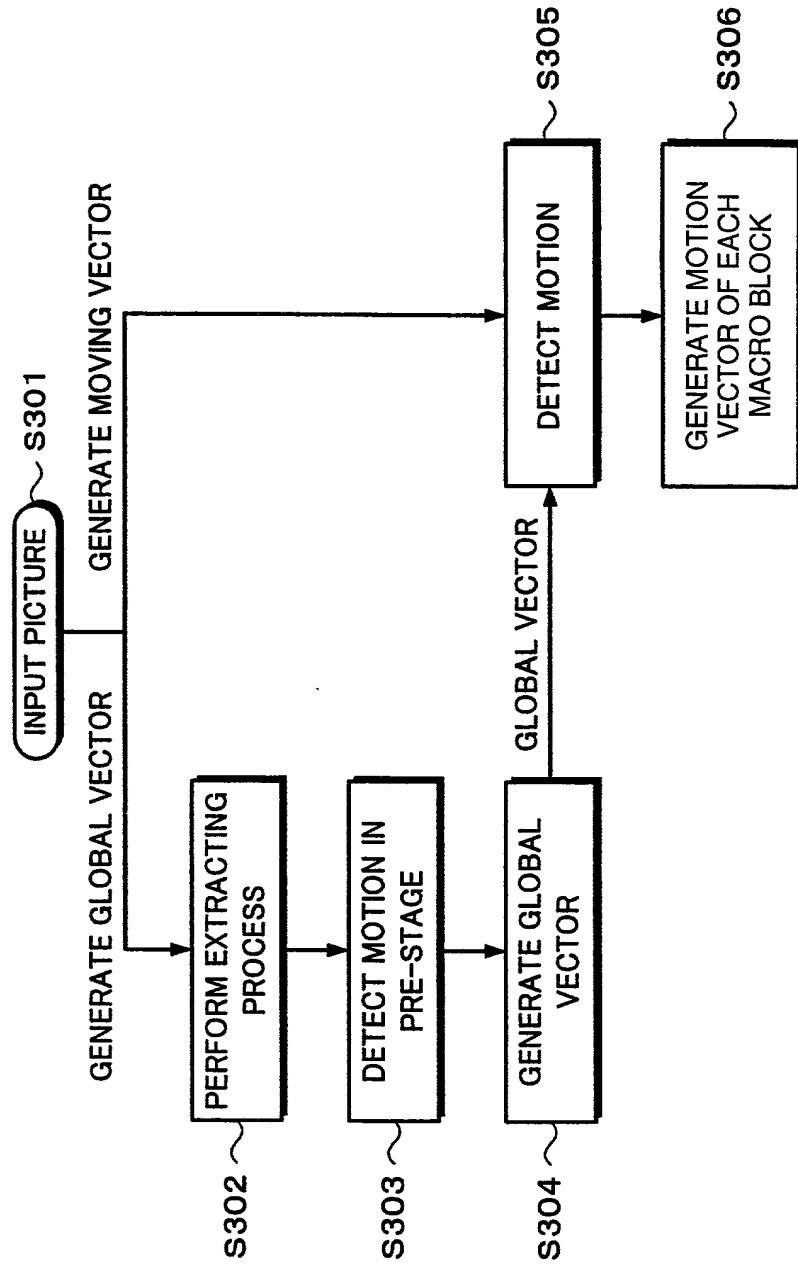


Fig. 31

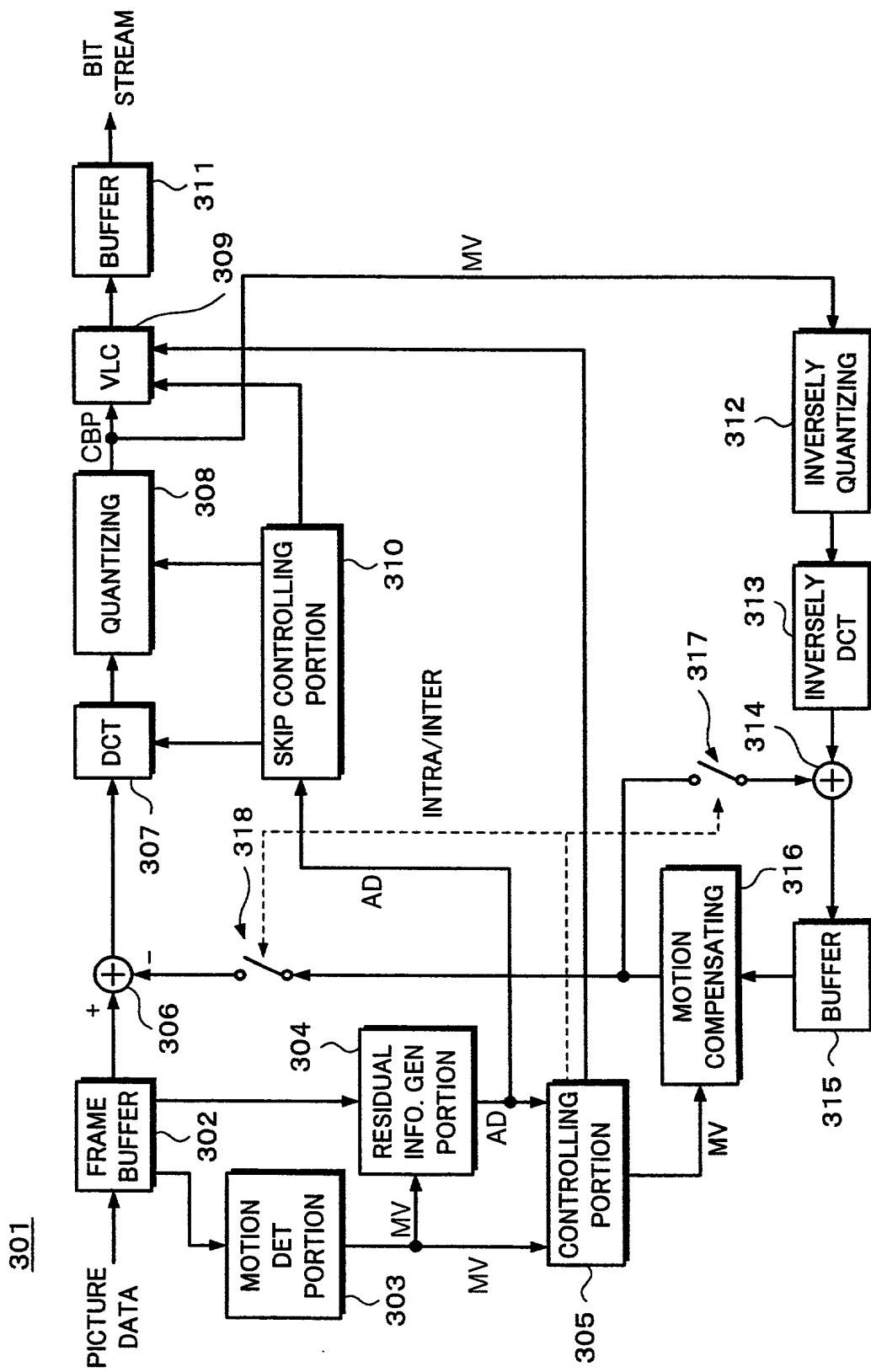


Fig. 32

